

GUJARAT TECHNOLOGICAL UNIVERSITY**B.E. Sem-III(Computer Engineering)Examination December/January 2009-10****Subject code: 130704****Subject Name: Computer Organization & Architecture****Date: 11 / 03 / 2010****Time: 03.00 pm – 05.30 pm****Total Marks: 70****Instructions:**

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

- Q.1 (a)** Define the following terms. **07**
- (i) Effective address
 - (ii) Immediate instruction
 - (iii) Register transfer language
 - (iv) Sequencer
 - (v) Computer organization
 - (vi) Pseudo instruction
 - (vii) Data Dependency
- (b)** Answer the following briefly
- (i) Explain selective set, selective complement and selective clear **02**
 - (ii) Show the block diagram of the hardware that implements the following register transfer statement . **03**
T2: R2 ← R1 , R1 ← R2
 - (iii) Explain one, two and three address instruction. **02**
- Q.2 (a)(i)** A digital computer has a common bus system for 16 registers of 32 bits each. **04**
- (i) How many selection input are there in each multiplexer?
 - (ii) What size of multiplexers are needed?
 - (iii) How many multiplexers are there in a bus?
- (ii)** Explain the following instructions **03**
- 1) CLA
 - 2) ISZ
 - 3) INP
- (b)** Explain 4 bit incrementer with a necessary diagram **07**
- OR**
- (b)** Explain Instruction cycle. **07**
- Q.3 (a)(i)** Write a note on subroutines. **04**
- (ii)** Explain Direct and Indirect Addressing **03**

- (b)(i) Write an assembly level program for the following pseudocode. **05**
 $SUM = 0$
 $SUM = SUM + A + B$
 $DIF = DIF - C$
 $SUM = SUM + DIF$
- (ii) Differentiate SIMD and MIMD. **02**
- OR**
- Q.3** (a) Show the contents of the registers E, A, Q, SC during the process of multiplication of two binary numbers 11111(multiplicand) 10101 (multiplier). The signs are not included. **07**
- (b)(i) Draw the space time diagram for six segment pipeline showing the time it takes to process 8 tasks. **04**
- (ii) Write a note on memory interleaving. **03**
- Q.4** (a)(i) Explain the characteristics of RISC and CISC. **05**
- (ii) Convert the following into reverse polish notation. **02**
- 1) $A+B*[C*D+E*(F+G)]$
2) $A*[B+C*(D+E)] / [F+G*(H+I)]$
- (b) Explain various types of interrupts **07**
- OR**
- Q.4** (a)(i) Explain overlapped windows register. **04**
- (ii) Explain the following terms **03**
- 1) PSW
2) Delayed load
3) Pipeline conflict
- (b) Explain Stack and evaluate the following expression using stack **07**
 $(3+4)*[10(2+6)+8]$
- Q.5** (a) Explain the first pass of an assembler with a flowchart **07**
- (b) Explain four types of instruction formats **07**
- OR**
- Q.5** (a) Explain booth algorithm for multiplication with a flowchart **07**
- (b) Write a note on different addressing modes **07**
